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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/961,202	09/24/2001	Baruch Solomon	2207/12173	6536

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/961,202	SOLOMON ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 3/1/2005.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 5-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamashiroya (US PAT. 6,470,425).

Regarding claim 5, Yamashiroya discloses a control method comprising on a cache hit, counting a number of accesses to a cache line that caused the hit, i.e., cache memory system comprising a hit/miss counter (300, figure 1) which counts the number of times a cache hit or miss occurs sequentially for each entry of the cache memory (col. 2 lines 33-40 and col. 2 line 44 through col. 3 line 8), if the count meets a predetermined threshold, enabling a segment builder, building and storing instruction segments from an output of the segment builder, i.e., cache memory system further comprising a hit threshold register (461, figure 3) wherein the hit threshold register contains number of sequential cache hits that is used as an update inhibition

condition for a cache memory entry, and when the number of sequential cache hits on an entry exceeds the number of times specified in the hit threshold register, the update of the entry is inhibited thereafter (col. 3 line 50 through col. 4 line 53).

Regarding claim 6, Yamashiroya discloses the control method further comprising if a hit also is registered in a segment cache, maintaining the segment builder disabled regardless of the count value (col. 4 lines 31-53).

Regarding claims 7-8, Yamashiroya discloses the control method further comprising if a hit also is registered in a segment cache, maintaining the segment builder disabled regardless of the count value, and incrementing the count value and storing the incremented count value in the cache line (col. 3 line 45 through col. 4 line 53).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashiroya (US PAT. 6,470,425) in view of Chauvel et al. (US PAT. 6,681,297 hereinafter Chauvel).

Regarding claims 9-10, Yamashiroya differs from the claimed invention in not specifically teaches the control method further comprising identifying a victim cache line, and reducing a count value of the victim cache line, and identifying an age of cache lines in a same set as the cache line that caused the hit, and reducing a count value of those cache lines that are older than a median age of all the cache lines in the same set. However, Chauvel teaches in the cache memory system comprising a miss counter to count each cache memory request miss corresponding to a monitored-qualifier value, and further comparing with the miss rate threshold to generate a flush command, and eviction the victim cache line based on a least recently use replacement algorithm (col. 13 line 61 through col. 14 line 63, col. 15 line 59 through col. 16 line 26 and col. 17 line 7 through col. 18 line 3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the cache control method of Yamashiroya having steps of comprising identifying a victim cache line, and reducing a count value of the victim cache line, and identifying an age of cache lines in a same set as the cache line that caused the hit, and reducing a count value of those cache lines that are older than a median age of all the cache lines in the same set, as per teaching by the cache memory system of Chauvel, because it minimizes eviction of useful entries of active tasks and thereby reduces power consumption.

6. Claims 11-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki (US PAT. 6,385,697) in view of Chauvel et al. (US PAT. 6,681,297 hereinafter Chauvel).

Regarding claim 11, Miyazaki discloses a instruction cache as shown in figure 5 comprising a plurality of entries comprising a tag field, a count field and a data field, an increment or (11, figure 6) coupled to the access count fields, and a threshold comparator (32, figure 5) coupled to the incrementor (11, figure 6 and col. 12 line 51 through col. 18 line 7). Although Miyazaki does not clearly discloses the instruction cache further comprising an address decoder and each indexed is output by the address decoder, Miyazaki teaches each of the entry received input address data, thus one skill in the art at the time the invention was made would recognize the input address data indexed by an output of an address decoder in response to executing certain instructions which may include parameters to specify the requested operation, as an example of Chauvel (col. 15 lines 45-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Miyazaki in having an address decoder and each indexed is output by the address decoder, as per teaching by Chauvel, because it minimizes eviction of useful entries of active tasks and thereby reduces power consumption.

Regarding claim 12, Miyazaki discloses the cache further comprising a tag comparator (30A and 30B, figure 5) coupled to the tag fields via bus, a transmission gate (31A, figure 5) coupled to the threshold comparator and controlled by an output from the tag comparator (figure 5 and col. 14 lines 10-26).

Regarding claim 13, Miyazaki discloses write control logic (33, figure 5) controlled by an output of the tag comparator (col. 15 line 66 through col. 16 line 9).

Regarding claims 14-15, Chauvel teaches in the cache memory system comprising a miss counter to count each cache memory request miss corresponding to a monitored-qualifier value, and further comparing with the miss rate threshold to generate a flush command, and eviction the victim cache line based on a least recently use replacement algorithm (col. 13 line 61 through col. 14 line 63, col. 15 line 59 through col. 16 line 26 and col. 17 line 7 through col. 18 line 3).

Regarding claim 16, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claim 17, the limitations of the claim are rejected as the same reasons set forth in claim 12.

Regarding claims 18-19, the limitations of the claims are rejected as the same reasons set forth in claims 14-15.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 13.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claims 22-23, Miyazaki discloses a instruction cache as shown in figure 5 comprising a plurality of entries comprising a tag field, a count field and a data field, an incrementor (11, figure 6) coupled to the access count fields, and a threshold comparator (32, figure 5) coupled to the incrementor.

Regarding claim 24, Miyazaki discloses a write controller (4, figure 6) coupled to an output of the incrementor (11, figure 6).

Regarding claim 25, Miyazaki discloses an output of the tag comparator enabling a segment builder (abstract).

Response to Arguments

7. Applicant's arguments filed 3/1/2005 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., instruction cache) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument that Yamashiroya contains no suggestion of any operation relating to instructions, it is noted that Yamashiroya teaches the cache memory system storing entries indicating whether or not the updated of the corresponding entry being inhibited, i.e., instruction segments (col. 3 lines 50-65). Note the claimed language fails to clearly define what the instruction segments are. Thus, Yamashiroya is enough to reject the broad claimed limitations. Correspondingly, claims 9 and 10 are also rejected under Yamashiroya and Chauvel for at least the reasons as stated in above.

8. Applicant's arguments with respect to claims 11-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Singh et al. (US PAT. 6,393,551) discloses reducing instruction transactions in a microprocessor (abstract).

Jourdan et al. (US PAT. 6,412,050) discloses memory record update filtering with a comparator can be in communication with the data tag field of the table memory and a data accessing information input to perform a data tag comparison (col. 2 lines 39-52).

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MATTHEW D. ANDERSON
PRIMARY EXAMINER

Zhuo H. Li

Patent Examiner
Art Unit 2189